IN THE CLAIMS:

1. (Amended) A built-in self-test controller, comprising:

a logic built-in self-test engine capable of executing a logic built-in self-test, including:

a logic built-in self-test state machine; and

a pattern generator seeded with a first primitive polynomial; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

2. (Original) The built-in self-test controller of claim 1, wherein the first primitive polynomial is $x^{31} + x^{3} + 1$.

3. (Original) The built-in self-test controller of claim 1, wherein the second primitive polynomial is $x^{32} + X^{28} + x + 1$.

4. (Original) The built-in self-test controller of claim 1, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and a done state entered into when the content of the pattern generator equals the predetermined vector count.

5. (Original) The built-in self-test controller of claim 1, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

6. (Original) The built-in self-test controller of claim 1, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done; a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

7. (Original) The built-in self-test controller of claim 1, wherein the seed for the pattern generator is externally configurable.

8. (Amended) A built-in self-test controller, comprising:

means for executing a logic built-in self-test, including a pattern generator seeded with a first primitive polynomial; and

means for storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

wherein the first polynomial has a first number of bits and the second polynomial has a second number of bits, wherein the second number is different from the first number.

9. (Original) The built-in self-test controller of claim 8, wherein the first primitive polynomial is $x^{31} + x^{3} + 1$.

10. (Original) The built-in self-test controller of claim 8, wherein the second primitive polynomial is $x^{32} + X^{28} + x + 1$.

11. (Original) The built-in self-test controller of claim 8, wherein the seed for the pattern generator is externally configurable.

12. (Amended) A integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof, including: a logic built-in self-test state machine; and a pattern generator seeded with a first primitive polynomial; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

13. (Original) The integrated circuit device of claim 12, wherein the first primitive polynomial is $x^{31} + x^{3} + 1$.

14. (Original) The integrated circuit device of claim 12, wherein the first primitive polynomial is $x^{32} + x^{28} + x + 1$.

15. (Original) The integrated circuit device of claim 12, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

16. (Original) The integrated circuit device of claim 12, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

17. (Original) The integrated circuit device of claim 12, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done; a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

18. (Original) The integrated circuit device of claim 12, further comprising: a memory built-in self-test engine; and

a memory built-in self-test signature register capable of storing the results of the memory built-in self-test.

19. (Original) The integrated circuit device of claim 12, wherein the memory components include a static random access memory device.

20. (Original) The integrated circuit device of claim 12, wherein testing interface comprises a Joint Test Action Group tap controller.

21. (Original) The integrated circuit device of claim 12, wherein the seed for the pattern generator is externally configurable.

22. (Amended) A method for performing a logic built-in self-test, the method comprising:

seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial; and

executing a logic built-in self-test using the contents of the pattern generator; and storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

23. (Original) The method of claim 22, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^{3} + 1$.

24. (Amended) The method of claim 23, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial ~~is~~ $x^{32} + x^{28} + x + 1$.

25. (Amended) The method of claim 22, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial ~~is~~ $x^{32} + x^{28} + x + 1$.

26. (Amended) The method of claim 22, wherein executing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of ~~the dual mode~~ the built-in self-test controller upon receipt of a logic built-in ~~selftest~~ self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of the pattern generator equals a predetermined vector count.

27. (Original) The method of claim 26, further comprising at least one of:

setting a bit in a multiple input signature register indicating whether the logic built-in self-test is done;

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

28. (Original) The method of claim 22, further comprising externally configuring the seed.

29. (Amended) A method for testing an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a logic built-in self-test, including:

seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial;

executing a logic built-in self-test using the contents of the pattern generator; and

storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial; and reading the stored results;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

30. (Original) The method of claim 29, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

31. (Amended) The method of claim 29, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial ~~is~~ $x^{32} + x^{28} + x + 1$.

32. (Original) The method of claim 29, further comprising externally configuring the seed.

33. (Original) The method of claim 29, further comprising performing a memory built-in self-test.